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A Study On Double Gate Field Effect Transistor For Area And Cost Efficiency

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Abstract: **Proposal for a field effect transistor had been presented, with numerical device simulations to verify the title in every manner possible. The two transitional field effect transistors like pMOS and nMOS functions are simultaneously performed, working as one or as the other according to the voltage applied to the gate terminal. Increase in the circuit speed is observed when this technology is implemented on the device suggested with respect to the standard CMOS technology, presented a drastic reduction of number devices and associated parasitic capacitances. In addition to it IC obtained with the proposed device are fully compatible with the standard CMOS technology and the fabrication processes. Fabrication of Static Ram cells with three transistors only with minimum dimensions and a single bit line by saving silicon area and increasing the memory performance with respect to standard CMOS technologies. It is also presented that the fully compatible CMOS process can be used to successfully manufacture the new FET structure.**

Keywords: **Fabrication, Double Gate, MOSFET device, multifunctional MOS, TFT, CMOS Technology.**

I. INTRODUCTION

For past few decades the challenge for VLSI has been integration of an ever increasing number of devices with high yield and reliability. The law of Moore's has been achieved by dramatic scaling of MOSFET physical dimensions which led to gaining speed and density [1].The CMOS channel length is scaled to the nanometer regime for which the device begin to lose their insulating properties as the thermal injection and quantum- mechanical tunneling phenomenon [2]. Hence results to rapid rise of the standby power of the chip. When a limit is placed on the integration level as well as on the switching speed for which a pessimistic predictions concerns the rate of technology process for semiconductor industry [3]. To follow the Moore's law new device structure had been proposed like double gate SOI MOSFET, D-channel MOSFET [4] [5] perhaps these device requires more complex process technology but lacks in scalability [6]. In this article an alternative approach to sustain the speed and density rate of modern integrated circuits [7], but in this approach i.e. the proposal as stated in this work is based on increasing the functions of an individual MOSFET device neither by shrinking its dimensions nor by adding more gates. By implementing the proposal as explained in these paper a series of device can be produced, but in here the area had been constricted to Double Gate FET, which is having two functionality pMOS and nMOS. This result to save silicon area and increases the circuit speeds.

II. STRUCTURE OF THE DEVICE

Fig.1 illustrated the cross -section structure of bulk double gate field effect transistor and this device is designed from a bulk MOSFET by adding extra p-doped poly layer on the top of this device. For obtain the proper functionality of this device, one of the n+ regions should be short circuited by the metal contact with one of the upper p+ regions in extra poly layer. The extra p-poly layer has been doped for the formation of junction-less Thin Film Transistor (TFT) module on the top of the MOSFET, as the final device is able to behave like an inverter or buffer rather than a bulk MOSFET. The gate of the device controls at the same time as the conductivity of the upper and lower channels enables the switching from the nMOS to the pMOS behavior depending on the voltage which is applied to the gate terminal. The complementary

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structure is also obtained by simply replacing the p-doped region with n-doped region and vice versa and this device is formed by a p-channel MOS, whereas the Thin Film Transistor module behaves as a n-channel transistor. Normally for obtained higher performance epitaxial silicon layer is used instead of poly-layer. Here in this case the single crystalline silicon layer can be formed by using an epitaxial lateral overgrowth technique [8] where the single crystalline silicon seed is growth through the metal contact by using undoped Selective Epitaxial Growth (SEG) process. This can be carried out at less than 700^0C by applying any one of the $H_2/SiH_4/Cl_2$ gas system. The alternative way is to use a Leaser-induced Epitaxial Growth (LEG) technology [9], [10].

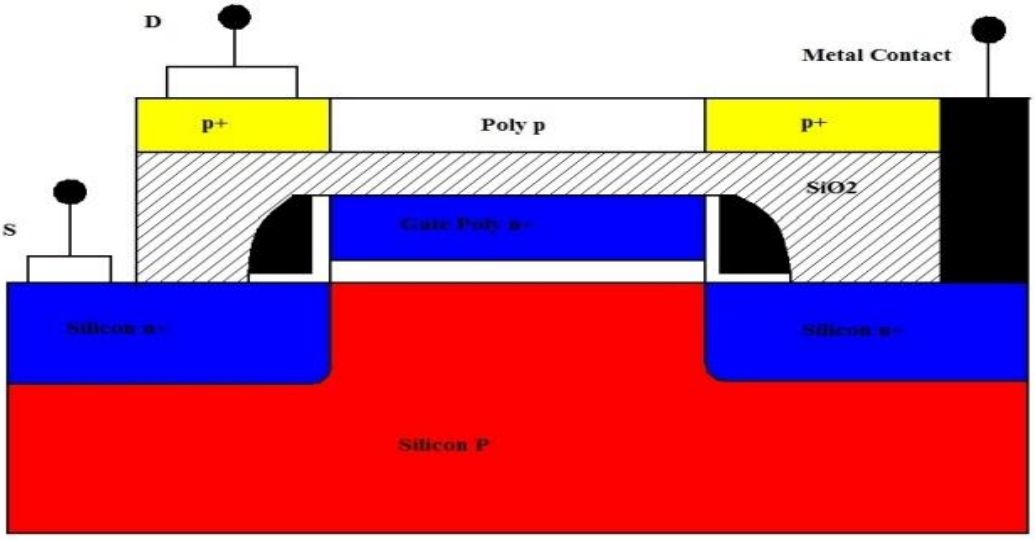


Fig.1 Structure of a Bulk Double Gate Field Effect Transistor

III. MODE OF OPERATION

The operation mode of the double gate controlled field effect transistor consider the situation in which the S (source) terminal is connected to ground D(drain) terminal is connected to V_{DD}.

When the gate voltage is less than the threshold voltage i.e. V_{tn} ($Vg<V_{tn}$), whereas the p-doped poly layer on the top of the gate allowing current to flow from the supply voltage to the output terminal. So the device behaves like a p-channel fully Depleted SOI device with the Drain terminal as a source and metal contact as a drain.

When gate voltage (V_g) increases, the upper poly layer deplete until the p channel is completely pinched off, and the electron channel under the lower gate - oxide increases. The width W_d of the depletion region is greater than the thickness X_t of the poly layer when Vg is beyond the threshold voltage. This results the metal terminal is isolated from the supply and the device behaves as a bulk n-channel MOS.

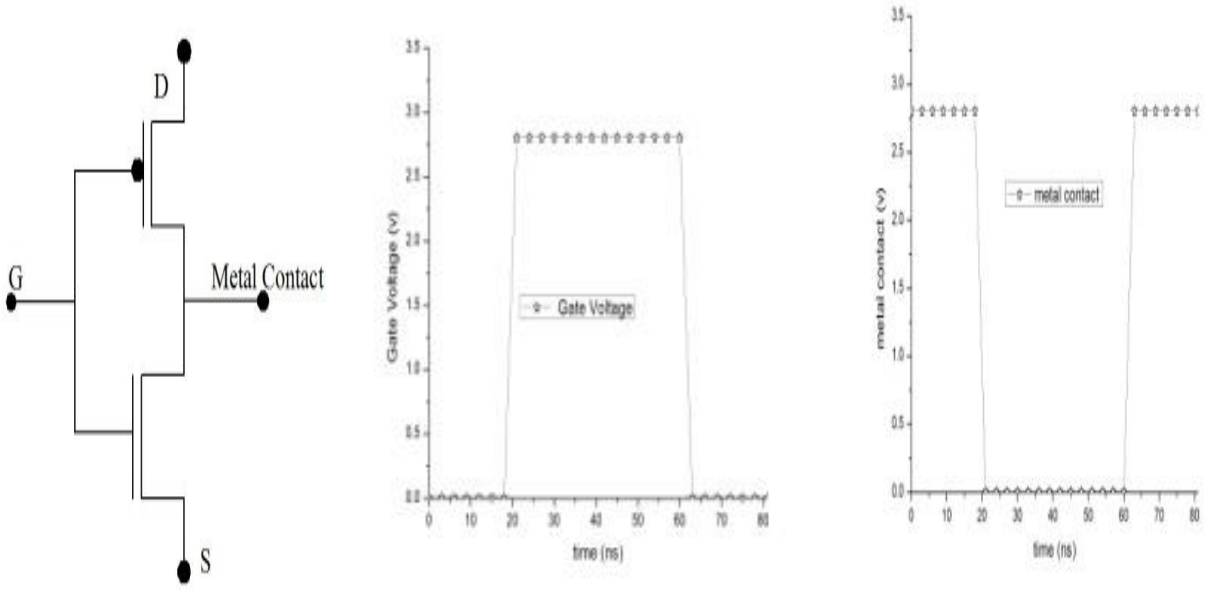
The upper Thin Film Transistor module to behave as an enhancement device rather than a depletion p channel Field Effect Transistor if the combination of the chosen gate work function with relatively small thickness of the extra poly layer , applied as such allows for the turning off of the device for relatively low gate values. The threshold voltage value increases towards negative values, which enables the enhancement mode behavior by using n+ doped gate instead of P+ doped gate

IV. NUMERICAL SIMULATION

Double Gate FET operates as two enhancements n-channel and p-channel MOS, which are connected as shown in the fig 2.a. for more emphasis in fig 2.b. the simulation, had been carried out using Sentaurus (Synopsys) [11]. A rectangular voltage is applied to the gate i.e. drain terminal to V_{DD} and the source terminal connected to ground, the device behaves as an inverter at the metal contact terminal which shows an inverted signal with respect to one of the applied to gate.

The proposed device consists of a bulk 0.18µm nMOS with a junction less TFT module. Furthermore there is a poly-silicon of 100nm thick p-doped with boron concentration of $10^{16}cm^{-3}$, the upper and lower gate of 5.2nm thickness. Hole

assumed for a poly-silicon with mobility of $9cm^2/Vs$ [12], the mobility of TFT device with gate oxide of 5.3nm is in order of $30cm^2/Vs$ [13]. Parameters like doping-dependent degradation, degradation due to high electric fields and interface effects during the simulation. There are two types of threshold voltages of double gate nMOS are V_{tn} and V_{tp}, when V_G is less than V_{tp} behaves like a pMOS device with drain terminal as a source and hence the current goes from the drain terminal to the metal contact terminal, in case where V_G is greater than V_{tn} the device behaves as a bulk nMOS and hence the current flows between the metal contact and the source terminals.



(a) (b)

Fig.2 nMos Double gate equivalent circuit (a), and TCAD device simulation results (b) obtained by applying a rectangular voltage pulse to the gate of a Double Gate device drain at 2.8V and source connected to ground. The solid line shows the behavior of the metal contact terminal.

V. FABRICATION AND EXPERIMENTAL RESULTS

The results from the simulations have shown that double gate FET was realized in 1.5µm CMOS technology with a 9 mask fabrication process

A. Fabrication Samples:

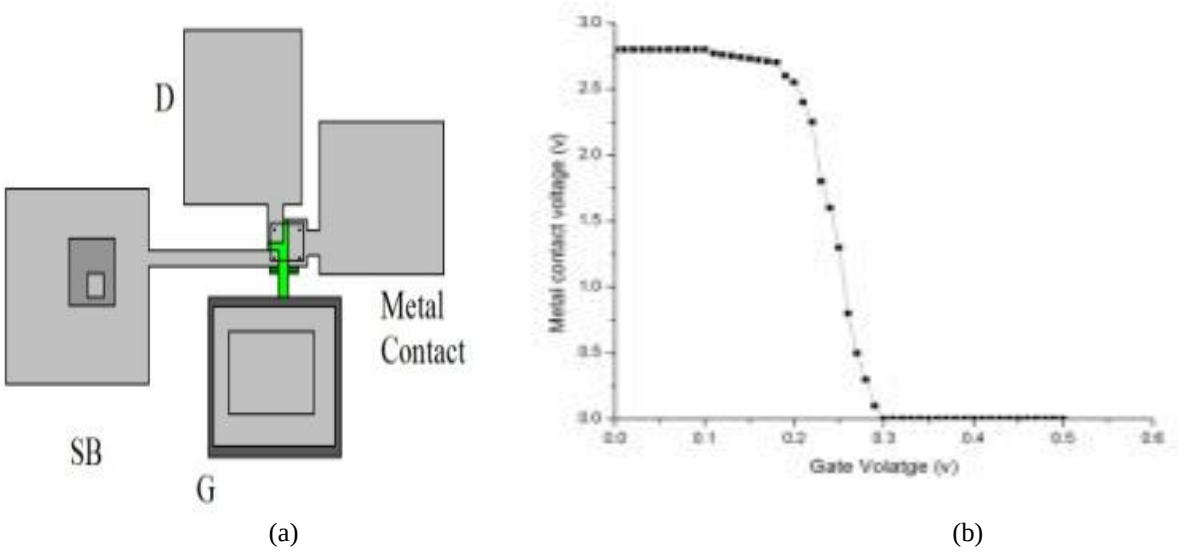
The device structure analyzed where p-doped silicon substrate of resistivity of 50-70 Ωcm, a p-well had been created with 2 X $10^{13}cm^{-2}$ with boron implant at 60keV for hosting the devices. In account of n^+ type regions are formed with a 2 X $10^{15}cm^{-2}$ with arsenic implant at 110keV. The gate is of poly-silicon doped with 8 X$10^{15}cm^{-2}$ phosphorus implant at 80keV. The poly gate formation and self-aligned n^+ implant and poly re-oxidation a thin 100nm a Si Layer deposited at 550^0C. The layer is implanted with Boron ($10^{12}cm^{-2}$ BF_2 at 50 keV) to form a channel above the underlying poly gate in addition to it a poly gate is etch used thereafter to define the device. The p^+ contacts are simultaneously formed with other p type layers with a $2X10^{15}cm^{-2}$ BF_2 implant at 80 keV. Top and bottom of gate oxides thickness are 11nm and 21.5nm respectively as indicated by ellipsometric measurements.

Fig 3a is the final result of the fabrication process, where the source and body terminals of device have shorted together marked by SB i.e. the source terminal.

B. Results of Experiment:

When voltage is supplied to drain terminal i.e. V_{DD} and the source (source and body terminals shorted) terminal connected to ground. As shown in the Fig 3b. In this condition the device behaves as an inverter at the metal contact terminal an

inverted signal with respect to the one applied to the gate. The gain measured of the device for supply voltage 1.5V was greater than 40 in absolute value, the short circuit current is 5 X 10^{-11}A/µm, whereas the measured steady state leakage is in the order of 3.6 X 10^{-14} A/µm which is very considering the utilized process Technology.



(a) (b)

Fig. 3. Micrograph of 1.5µm Double Gate MOS device (a) and DC measurements of the metal contact terminal voltage as a function of the gate voltage in inverter mode (b), i.e. with the SB(Source Body) terminal connected to ground and drain at 2.8V

VI. CONCLUSIONS

In this work the device proposed seems to be an alternative approach focusing on increase the functions of a single device rather than shrinking the dimensions of a bulk MOSFET or adding more control gates with a very complicated process technology. The simulation results showed the electrical characteristics and details fabrication process which also explains a fully compatible CMOS process can be used to successfully manufacture the new FET structure. Numerical Based simulations showed details about the double gate FET behavior and the correlations existing between the different geometrical and physical parameters of the device.

The proposed technology will also enable the fabrication of Static RAM cells with only 3 transistors rather than 6, with minimum dimensions and single bit line, saving silicon area and increasing the memory performance in comparison with the bulk CMOS technologies. It is also observed that combinational and sequential circuits using the proposed method, with respect to CMOS show a drastic decrease of both device number and parasitic capacitances which results to improvement of the circuit speed.

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